A3 cont'd.

geometries of the printed circuit inductor 30 and printed circuit capacitor conductor 40 to realize series resonance at 400 MHz. In order to trade inductor to resonant at 400 MHz, simulation indicated that a 2.7 inches trace length (L), 5 mils trace width (W), 5 mils trace space (S), and three turns (N). The tuning capacitor was formed as a square, approximately 135 mils x 135 mils. When the serpentine trace resonants at 400 MHz, a low impedance path from the discrete capacitor's power pad to the ground plane (under the serpentine trace on the board) is effected, and the 400 MHz noise is substantially attenuated.

Please replace the paragraph beginning on Page 11, line 1 with the following amended paragraph:

A4

The Detailed Description, insofar as provided above, has elaborated a specific embodiment of the invention in generous detail, so as to enable a skilled artisan to understand and exploit the invention. However, certain ramifications of the invention are worthy of elaboration. In particular, the LC network has been described as including an inductance 30 and a tuning capacitance conductor 40. To be rigorously precise, as distributed circuit elements, there is both a quantum of capacitance associated with conductor 30 and a quantum of inductance associated with conductor 40. However, at a frequency of interest, F_o, conductor 30 is predominantly inductive and conductor 40 is predominantly capacitive. In this regard (inductive) conductor 30 is particularly described as having a serpentine geometry. However, the invention comprehends other geometries that, at a predetermined F_o, exhibit an inductive impedance. A serpentine conductor results in an inductance at high frequencies, in large part, because of the directional changes necessarily imparted to the current flowing through it. Similarly (capacitive) conductor 40 invites other geometries as well, and a rectangular perimeter is propounded largely for simplicity and regularity. Those skilled in the art realize that the resulting capacitance of conductor 40 is largely dependent on the area subtended by the conductor, the thickness of the PCB 101, and its dielectric properties.

In the Claims

The following is a clean version of the entire set of pending claims. In accordance with 37 CFR § 1.121(c)(1)(ii), Attachment A provides marked up versions of the claims containing the newly introduced changes.

Q5

1. (Amended) A circuit board having a power supply and a ground, the circuit board comprising:

a first conductive pad interfaced with the power supply of the circuit board;

a second conductive pad interfaced with the ground of the circuit board;

a capacitive element connected between the first and the second conductive pads; and

a series-resonant impedance coupled to the first pad, the series-resonant impedance comprising a serpentine conductor deposited on the circuit board and a tuning capacitance deposited on the circuit board.

2. (As Filed) A circuit board as defined in Claim 1, wherein the serpentine conductor is formed from a conductor that is printed on the circuit board.

3. (As Filed) A circuit board as defined in Claim 2, wherein tuning capacitance is planar in form.

4. (As Filed) A circuit board as defined in Claim 3, wherein the tuning capacitance is printed on the circuit board.

5. (As Filed) A circuit board as defined in Claim 1, wherein the serpentine conductor comprises:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segments.

6. (Amended) A circuit board as defined in Claim 1, wherein serpentine conductor comprises:

at least one intermediate linear segment;

a first turn coupling the originating segment to the at least one intermediate linear segment;

a second turn coupling the first linear segment to an intermediate linear segment; and

a second turn coupling an intermediate linear segment to the second linear segment.

7. (Amended) A circuit board as defined in Claim 6, wherein the serpentine conductor has a length (L) and a width (W) and wherein the respective lengths of the turns establishes a space (S) between adjacent linear segment and wherein the number of turns is equal to N, and wherein S, L, W and N are chosen so that the serpentine conductor is at least approximately series resonant with the tuning capacitance at a significant frequency F_0.

Q5 cont'd

8. (As Filed) A circuit board as defined in Claim 7, wherein the tuning capacitance is substantially rectangular.

9. (As Filed) A circuit board as defined in Claim 8, wherein the linear segments are respectively mutually parallel.

10. (Amended) A computer system comprising:

a printed circuit board;

at least one integrated circuit device mounted on the printed circuit board, the integrated circuit device having a significant frequency, F_o;

an active conductor coupled to the integrated circuit device;

a reference conductor coupled to the integrated circuit device;

a first pad coupled to the active conductor;

a second pad coupled to the reference conductor;

a capacitor coupled between the first pad and the second pad; and

means coupled to the capacitor for attenuating signals at F_o, the means comprising a serpentine conductor and a tuning capacitance, the serpentine conductor and tuning capacitance deposited on the printed circuit board.

11. (As Filed) A computer system as defined in Claim 10, wherein the reference conductor provides a ground potential to the integrated circuit device.

12. (As Filed) A computer system as defined in Claim 11, wherein the active conductor supplies an operating voltage to the integrated circuit device.

13. (As Filed) A computer system as defined in Claim 11, wherein the active conductor supplies an operating signal to the integrated circuit device.

14. (As Filed) A computer system as defined in Claim 10, wherein tuning capacitance is printed on the circuit board in the form of a substantially rectangular plane.

15. (As Filed) A computer system as defined in Claim 14, wherein the tuning capacitance is coupled to the reference conductor.

Q5 cont'd.

16. (As Filed) A computer system as defined in Claim 14, wherein the serpentine conductor is printed on the printed circuit board.

17. (Amended) A computer system as defined in Claim 14, wherein the serpentine conductor comprises:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segment.

18. (Amended) A computer system as defined in Claim 17, wherein serpentine conductor comprises:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment; and

the second turn coupling an intermediate linear segment to the second linear segment.

19. (Amended) A computer system as defined in Claim 18, wherein the serpentine conductor has a length (L) and a width (W) and the respective lengths of the turns establishes the space (S) between adjacent linear segments and wherein the number of turns is equal to N, and

wherein S, L, W and N are chosen so that the serpentine conductor is at least approximately series resonant with the capacitance at a significant frequency F_o.

20. (Cancel without prejudice or disclaimer.)

21. (Amended) A computer system as defined in Claim 20, wherein the linear segments are respectively mutually parallel.

22. (As Filed) A method of enabling the suppression of spurious signals in electronic equipment, the method comprising:

attaching a discrete capacitor to a printed circuit board (PCB) between a power pad and a reference pad;

depositing an inductance on the PCB so that the inductance is connected at a first end to the power pad;

forming a tuning capacitance on the PCB so that the tuning capacitance is connected to a second end of the inductance; and

causing the inductance and tuning capacitance to be dimensioned so that the inductance and tuning capacitance are substantially series resonant at a predetermined frequency, F_o.

23. (As Filed) A method as defined in Claim 22, wherein the inductance is deposited to form:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segments.

24. (Amended) A method as defined in Claim 23, wherein the inductance is deposited to form:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

the second turn coupling an intermediate linear segment to the second linear segment;

and

a third turn coupling an intermediate segment to the second trace.

25. (As Filed) A method as defined in Claim 24, wherein the inductance is deposited in a manner so that:

(i) the inductance has a length (L) and a width (W);

(ii) respective lengths of the turns establishes a space (S) between adjacent linear segments;

(iii) the number of turns is equal to (N); and

(iv) S, L, W, S and N establish a magnitude of the inductance such that the inductance is at least approximately series resonant with the tuning capacitance at F_o.

Cl 5 cont'd.

26. (As Filed) A method as defined in Claim 23, wherein the tuning capacitance is formed by depositing a planar conductor on a first surface of the PCB and positioning the planar conductor in proximity with a ground plane.

27. (Amended) A method as defined in Claim 26, wherein the inductance is deposited to form:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

the second turn coupling an intermediate linear segment to the second linear segment;

and

a third turn coupling an intermediate segment to the second linear segment.

28. (As Filed) A method as defined in Claim 25, wherein the inductance is deposited in a manner so that:

(i) the inductance has a length (L) and a width (W);

(ii) respective lengths of the turns establishes a space (S) between adjacent linear traces;

(iii) the number of turns is equal to (N); and

(iv) S, L, W, S and N establish a magnitude of the inductance such that the inductance is at least approximately series resonant with the tuning capacitance at F_o.

29. (As Filed) In an electronic equipment, a circuit for attenuating spurious signals at high frequencies, the circuit comprising:

a power pad;

a reference pad;

a discrete capacitor coupled between the power pad and the reference pad;

a ground plane; and

a printed circuit LC network connected to the power pad and coupled to the ground plane, and resonant at a predetermined frequency of a spurious signal, the LC network comprising:

a capacitive element;

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the power pad;

a terminating segment coupling a second linear segment to the capacitive element; and

a turn coupling two adjacent linear segments.

30. (Amended) A circuit as defined in Claim 29, wherein the LC network further comprises:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

the second turn coupling an intermediate linear segment to the second linear segment; and

a third turn coupling an intermediate segment to the second linear segment.

31. (As Filed) A circuit as defined in Claim 29, wherein the capacitive element is formed by affixing a planar conductor on a first surface of a printed circuit board in proximity with the ground plane.

32. (As Filed) A circuit as defined in Claim 31, wherein the ground planes is affixed to a second surface of the printed circuit board.

33. (Amended) A circuit as defined in Claim 31, wherein the LC network further comprises:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

the second turn coupling an intermediate linear segment to the second linear segment; and

a third turn coupling an intermediate segment to the second linear segment.

cont'd.

34. (As Filed) A circuit as defined in Claim 34, wherein the linear segments are mutually substantially parallel.

35. (As Filed) A circuit as defined in Claim 33, wherein the printed circuit LC network comprises a number, N, substantially linear segments, each having a width, W, and mutually-spaced from an adjacent linear segment by a distance, S, where N, W and S are chosen to form an inductance that in combination with the capacitive element and the discrete capacitor effects substantial attenuation at the predetermined frequency.

36. (Amended) In an electronic equipment, a circuit module comprising:

a printed circuit board having a top surface and a bottom surface, the printed circuit board formed from a dielectric material having a thickness;

a first conductive pad deposited on a surface of the printed circuit board;

a second conductive pad deposited on a surface of the printed circuit board;

a ground plane;

a capacitor coupled between the first and the second conductive pads; and

means, including an inductance and a capacitance, coupled to the first pad for suppressing spurious signals at a predetermined frequency, the capacitance formed by a conductor deposited on a surface of the printed circuit board and separated from the ground plane by the printed circuit board to have a predetermined tuning capacitance set by the printed circuit board dielectric thickness.

37. (As Filed) A circuit module as defined in claim 36, wherein the means consists essentially of a conductive trace disposed on the printed circuit board.

38. (Amended) A circuit module as defined in Claim 36, wherein the means comprises:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segments.

Cl 5 cont'd.

39. (Amended) A circuit module as defined in Claim 38, wherein the means comprises:

at least one intermediate linear segment;

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment; and

a third turn coupling an intermediate linear segment to the second linear segment.

This submission cancels Claim 20 and amends Claims 1, 6, 7, 10, 17-19, 21, 24, 27, 30, 33, 36, 38, and 39. In accordance with 37 CFR § 1.121(c)(1)(ii), Attachment A provides marked up versions of the claims containing the newly introduced changes.

REMARKS

The Examiner has objected to the specification and claims and has rejected all pending claims. Applicants have amended the specification and claims and respectfully request reconsideration of the Examiner's objections and rejections and full allowance of all pending claims.

1. Objections to the Specification.

Applicants have amended the specification to clarify that conductor 40 acts to provide tuning capacitance as described on page 9 at line 24. Applicants respectfully submit that no new matter has been introduced by the amendments to the specification. Applicants respectfully request withdrawal of the objection to the written disclosure.

2. Objections to the Claims.

Applicants have amended Claims 7, 17-21 and 38 substantially as suggested by the Examiner and respectfully request withdrawal of the objections to the claims.

3. Claim Rejections Under Section 112, Second Paragraph.

Applicants have canceled Claim 20 and have amended Claims 6, 18, 24, 27, 30, 33, 34, 38 and 39 to address the informalities pointed out by the Examiner. Applicants respectfully request withdrawal of the rejections to the claims under Section 112, second paragraph.

4. Claim Rejections Under Section 102.

Claim 36 stands rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,016,084 issued to Sugimoto.

Claims 1, 10 and 22 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,717,359 issued to Matsui et al.

Sugimoto discloses a method for connecting a printed circuit board with a housing with Figure 11 depicting an embodiment in which a ground connects with a printed circuit board through three parallel RLC circuits.

Claim 36 as amended recites, in part, "means, including an inductance and a capacitance, coupled to the first pad for suppressing spurious signals at a predetermined frequency, the capacitance formed by a conductor deposited on a surface of the printed circuit board and separated from the ground plane by the printed circuit board to have a predetermined tuning capacitance set by the printed circuit board dielectric thickness."

Sugimoto cannot anticipate Claim 36 since Sugimoto fails to teach, disclose or suggest all elements recited by Claim 36. For instance, Sugimoto fails to teach, disclose or suggest "capacitance formed by a conductor deposited on a surface of the printed circuit board and separated from the ground plane by the printed circuit board to have a predetermined tuning capacitance set by the printed circuit board dielectric thickness." Sugimoto instead discloses chip type capacitors. Accordingly, Applicants respectfully submit that Claim 36 is not anticipated by Sugimoto and respectfully request withdrawal of the rejection to Claim 36 and allowance of Claim 36 and Claims 37-39 which depend from Claim 36.

Matsui discloses a semiconductor integrated circuit with terminal pad connections that include a pad for a power source and ground. Figure 5 of Matsui discloses an equivalent circuit diagram of the semiconductor integrated circuit.

Claim 1 as amended recites, in part, a "circuit board" comprising "a series-resonant impedance coupled to the first pad, the series-resonant impedance comprising a serpentine conductor deposited on the circuit board and a tuning capacitance deposited on the circuit board."

Claim 10 as amended recites, in part, "means coupled to the capacitor for attenuating signals at F_o, the means comprising a serpentine conductor and a tuning capacitance, the serpentine conductor and tuning capacitance deposited on the printed circuit board."

Claim 22 recites, in part, a method comprising "depositing an inductance on the PCB" and "forming a tuning capacitance on the PCB."

Matsui cannot anticipate Claims 1, 10 or 22 because Matsui fails to teach, disclose or suggest all elements recited by Claims 1, 10 and 22. For instance, Matsui fails to teach, disclose or suggest a circuit board or a printed circuit board as recited by Claims 1, 10 and 22. Matsui also fails to teach, disclose or suggest "a serpentine conductor deposited on the circuit board and a tuning capacitance deposited on the circuit board" as recited by Claim 1. Matsui fails to teach, disclose or suggest a "serpentine conductor and tuning capacitance deposited on the printed circuit board" as recited by Claim 10. Matsui fails to teach, disclose or suggest a method of "depositing an inductance on the PCB" and "forming a tuning capacitance on the PCB" as recited by Claim 22. Accordingly, Applicants respectfully request that the Examiner withdraw the rejections of Claims 1, 10 and 22 and the rejections to Claims 2-9, 11-19 and 21, and 22-28 which depend from Claims 1, 10 and 22 respectively.

5. *Rejections under Section 103.*

Claim 1 stands rejected under 35 U.S.C. § 103 as being unpatentable over Sugimoto.

Claim 29 stands rejected under 35 U.S.C. § 103 as being unpatentable over Matsui in view of U.S. Patent No. 6,061,222 issued to Morris et al.

Sugimoto cannot make obvious Claim 1 because Sugimoto fails to teach, disclose or suggest all elements recited by Claim 1. Sugimoto discloses an RLC circuit disposed between the ground of a printed circuit board and conductive part of a housing. In contrast, Claim 1 recites a capacitive element connected between a first conductive pad associated with a power supply and a second conductive pad associated with a ground. Claim 1 also recites a series-resonant impedance coupled to the first pad. Sugimoto fails to teach disclose or suggest placing an RLC circuit between a power conductive pad and ground conductive pad. Sugimoto also fails to disclose separate capacitive element circuit and series-resonant impedance circuit. Accordingly, Sugimoto cannot make obvious Claim 1 and Applicants respectfully request that the Examiner withdraw the rejection of Claim 1 and Claims 2-9 which depend from Claim 1.

Matsui and Morris, considered either separately or in combination, cannot make obvious Claim 29 because Matsui and Morris fail to teach, disclose or suggest all elements recited by Claim 29. For instance, Claim 29 recites, in part, a "printed circuit LC network." Both Matsui

and Morris disclose circuits built into an integrated circuit semiconductor device. Accordingly, Matsui and Morris cannot make obvious Claim 29 and Applicants respectfully request that the Examiner withdraw the rejection of Claim 29 and Claims 30-35 which depend from Claim 29.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being transmitted via facsimile to: COMMISSIONER FOR PATENTS, Washington, D.C. 20231, on December 3, 2002.

Attorney for Applicant(s) — 3 Dec 2002 Date of Signature

Respectfully submitted,

Robert W. Holland
Attorney for Applicant(s)
Reg. No. 40,020

APPENDIX A

The following is a "Marked Up" version of the entire set of claims showing the changes that the accompanying submission makes to the claims of Serial No. 09/931,229:

1. (Amended) A circuit board having a power supply and a ground, the circuit board comprising:

a first conductive pad interfaced with the power supply of the circuit board;

a second conductive pad interfaced with the ground of the circuit board;

a capacitive element connected between the first and the second conductive pads; and

a series-resonant impedance coupled to the first pad, the series-resonant impedance comprising a serpentine conductor deposited on the circuit board and a tuning capacitance deposited on the circuit board.

2. (As Filed) A circuit board as defined in Claim 1, wherein the serpentine conductor is formed from a conductor that is printed on the circuit board.

3. (As Filed) A circuit board as defined in Claim 2, wherein tuning capacitance is planar in form.

4. (As Filed) A circuit board as defined in Claim 3, wherein the tuning capacitance is printed on the circuit board.

5. (As Filed) A circuit board as defined in Claim 1, wherein the serpentine conductor comprises:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segments.

6. (Amended) A circuit board as defined in Claim 1, wherein serpentine conductor comprises:

at least one intermediate linear segment;

a first turn coupling the originating segment to the [first] at least one intermediate linear segment;

a second turn coupling the first linear segment to an intermediate linear segment; and

a second turn coupling an intermediate linear segment to the second linear segment.

7. (Amended) A circuit board as defined in Claim 6, wherein the serpentine conductor has a length (L) and a width (W) and wherein the respective lengths of the turns establishes a space (S) between adjacent linear segment and wherein the number of turns is equal to N, and wherein S, L, W and N are chosen so that the serpentine conductor is at least approximately series resonant with the tuning capacitance at a significant frequency [F°] F_0.

8. (As Filed) A circuit board as defined in Claim 7, wherein the tuning capacitance is substantially rectangular.

9. (As Filed) A circuit board as defined in Claim 8, wherein the linear segments are respectively mutually parallel.

10. (Amended) A computer system comprising:

a printed circuit board;

at least one integrated circuit device mounted on the printed circuit board, the integrated circuit device having a significant frequency, F_o;

an active conductor coupled to the integrated circuit device;

a reference conductor coupled to the integrated circuit device;

a first pad coupled to the active conductor;

a second pad coupled to the reference conductor;

a capacitor coupled between the first pad and the second pad; and

means coupled to the capacitor for attenuating signals at F_o, the means comprising a serpentine conductor and a tuning capacitance, the serpentine conductor and tuning capacitance deposited on the printed circuit board.

11. (As Filed) A computer system as defined in Claim 10, wherein the reference conductor provides a ground potential to the integrated circuit device.

12. (As Filed) A computer system as defined in Claim 11, wherein the active conductor supplies an operating voltage to the integrated circuit device.

13. (As Filed) A computer system as defined in Claim 11, wherein the active conductor supplies an operating signal to the integrated circuit device.

14. (As Filed) A computer system as defined in Claim 10, wherein tuning capacitance is printed on the circuit board in the form of a substantially rectangular plane.

15. (As Filed) A computer system as defined in Claim 14, wherein the tuning capacitance is coupled to the reference conductor.

16. (As Filed) A computer system as defined in Claim 14, wherein the serpentine conductor is printed on the printed circuit board.

17. (Amended) A [circuit board] computer system as defined in Claim 14, wherein the serpentine conductor comprises:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segment.

18. (Amended) A [circuit board] computer system as defined in Claim 17, wherein serpentine conductor comprises:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment; and

the [a] second turn coupling an intermediate linear segment to the second linear segment.

19. (Amended) A [circuit board] computer system as defined in Claim 18, wherein the serpentine conductor has a length (L) and a width (W) and the respective lengths of the turns establishes the space (S) between adjacent linear segments and wherein the number of turns is equal to N, and wherein S, L, W and N are chosen so that the serpentine conductor is at least approximately series resonant with the capacitance at a significant frequency F_o.

20. (Cancel without prejudice or disclaimer.)

21. (Amended) A [circuit board] computer system as defined in Claim 20, wherein the linear segments are respectively mutually parallel.

22. (As Filed) A method of enabling the suppression of spurious signals in electronic equipment, the method comprising:

attaching a discrete capacitor to a printed circuit board (PCB) between a power pad and a reference pad;

depositing an inductance on the PCB so that the inductance is connected at a first end to the power pad;

forming a tuning capacitance on the PCB so that the tuning capacitance is connected to a second end of the inductance; and

causing the inductance and tuning capacitance to be dimensioned so that the inductance and tuning capacitance are substantially series resonant at a predetermined frequency, F_o.

23. (As Filed) A method as defined in Claim 22, wherein the inductance is deposited to form:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segments.

24. (Amended) A method as defined in Claim 23, wherein the inductance is deposited to form:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

the [a] second turn coupling an intermediate [trace] linear segment to the second [trace] linear segment; and

a third turn coupling an intermediate segment to the second trace.

25. (As Filed) A method as defined in Claim 24, wherein the inductance is deposited in a manner so that:

(i) the inductance has a length (L) and a width (W);

(ii) respective lengths of the turns establishes a space (S) between adjacent linear segments;

(iii) the number of turns is equal to (N); and

(iv) S, L, W, S and N establish a magnitude of the inductance such that the inductance is at least approximately series resonant with the tuning capacitance at F_o.

26. (As Filed) A method as defined in Claim 23, wherein the tuning capacitance is formed by depositing a planar conductor on a first surface of the PCB and positioning the planar conductor in proximity with a ground plane.

27. (Amended) A method as defined in Claim 26, wherein the inductance is deposited to form:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

the [a] second turn coupling an intermediate linear segment to the second linear segment; and

a third turn coupling an intermediate segment to the second linear segment.

28. (As Filed) A method as defined in Claim 25, wherein the inductance is deposited in a manner so that:

(i) the inductance has a length (L) and a width (W);

(ii) respective lengths of the turns establishes a space (S) between adjacent linear traces;

(iii) the number of turns is equal to (N); and

(iv) S, L, W, S and N establish a magnitude of the inductance such that the inductance is at least approximately series resonant with the tuning capacitance at F_o.

29. (As Filed) In an electronic equipment, a circuit for attenuating spurious signals at high frequencies, the circuit comprising:

a power pad;

a reference pad;

a discrete capacitor coupled between the power pad and the reference pad;

a ground plane; and

a printed circuit LC network connected to the power pad and coupled to the ground plane, and resonant at a predetermined frequency of a spurious signal, the LC network comprising:

a capacitive element;

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the power pad;

a terminating segment coupling a second linear segment to the capacitive element; and

a turn coupling two adjacent linear segments.

30. (Amended) A circuit as defined in Claim 29, wherein the LC network further comprises:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

the [a] second turn coupling an intermediate linear segment to the second linear segment; and

a third turn coupling an intermediate segment to the second linear segment.

31. (As Filed) A circuit as defined in Claim 29, wherein the capacitive element is formed by affixing a planar conductor on a first surface of a printed circuit board in proximity with the ground plane.

32. (As Filed) A circuit as defined in Claim 31, wherein the ground planes is affixed to a second surface of the printed circuit board.

33. (Amended) A circuit as defined in Claim 31, wherein the LC network further comprises:

at least one intermediate linear segment; and

plural turns comprising:

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

the [a] second turn coupling an intermediate linear segment to the second linear segment; and

a third turn coupling an intermediate segment to the second linear segment.

34. (As Filed) A circuit as defined in Claim 34, wherein the linear segments are mutually substantially parallel.

35. (As Filed) A circuit as defined in Claim 33, wherein the printed circuit LC network comprises a number, N, substantially linear segments, each having a width, W, and mutually-spaced from an adjacent linear segment by a distance, S, where N, W and S are chosen to form an inductance that in combination with the capacitive element and the discrete capacitor effects substantial attenuation at the predetermined frequency.

36. (Amended) In an electronic equipment, a circuit module comprising:

a printed circuit board having a top surface and a bottom surface, the printed circuit board formed from a dielectric material having a thickness;

a first conductive pad deposited on a surface of the printed circuit board;

a second conductive pad deposited on a surface of the printed circuit board;

a ground plane;

a capacitor coupled between the first and the second conductive pads; and

means, including an inductance and a capacitance, coupled to the first pad for suppressing spurious signals at a predetermined frequency, the capacitance formed by a conductor deposited on a surface of the printed circuit board and separated from the ground plane by the printed circuit board to have a predetermined tuning capacitance set by the printed circuit board dielectric thickness.

37. (As Filed) A circuit module as defined in claim 36, wherein the means consists essentially of a conductive trace disposed on the printed circuit board.

38. (Amended) A circuit module as defined in Claim [1] 36, wherein the means comprises:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segments.

39. (Amended) A circuit module as defined in Claim [39] 38, wherein the means comprises:

at least one intermediate linear segment;

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment; and

a third turn coupling an intermediate linear segment to the second linear segment.